Components for Energy-Efficient Operating Systems

Seminar “Selected Chapters of System Software Techniques: Energy-aware Systems”

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Motivation

Why?

- Battery technology stagnates
- CPUs and devices offer more and better power savings mechanisms

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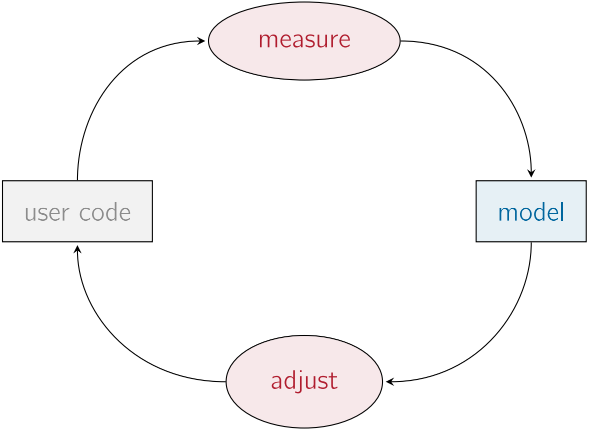
Question

How can operating systems be designed to efficiently use those mechanisms?

Outline



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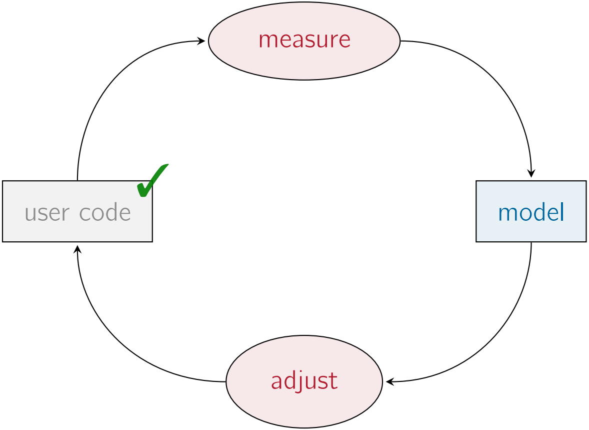

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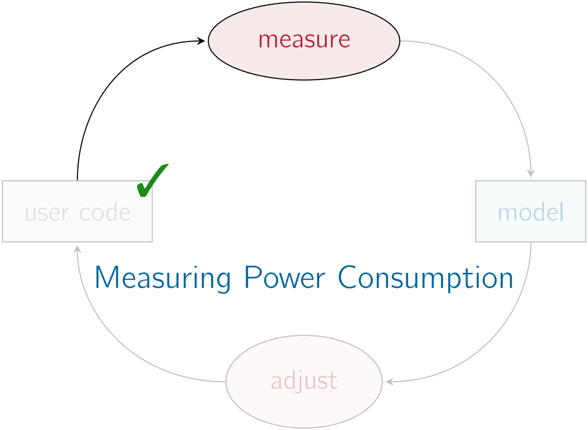

Measuring Power Consumption

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  - **Static power consumption**: power dissipation
  - **Dynamic power consumption**: transistor switching
- Can we influence static power usage?
  - If we can’t change it, do we still have to model it?
  - **Yes:** dynamic voltage scaling, factor in race-to-halt decisions

Identifying Key Power Consumers

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- **Devices**

  Not covered in this talk

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  - Current measurement equipment is not available in off-the-shelf systems
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- Solution: Estimate power usage using **event counters**
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  - Traditionally used for performance analysis
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    $\Rightarrow$ How can the ideal subset be chosen?
- Choosing subset of events
  - Run series of benchmarks with known behavior at all power saving configurations
  - Measure power consumption using dedicated hardware
  - Choose events correlating with power usage
  - **Note: hardware-specific!**

Maximizing Energy Efficiency: A Naïve Approach

$$\text{minimize} \quad \frac{\text{energy}}{\text{performance}} \left(= \frac{\text{power usage} \cdot \text{time}}{\text{time}^{-1}} = \text{power usage} \cdot \text{time}^2 \right)$$

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- Efficiency for
  - **CPU-bound** tasks: only little difference
  - **Memory-bound** tasks: higher efficiency at low speeds
- ⇒ run CPU-bound tasks at highest, memory-bound tasks at lowest speed
  - Low speeds significantly reduce performance
  - Users expect fast systems
  - **There is no free lunch:** performance vs. energy is a trade-off

No Free Lunch

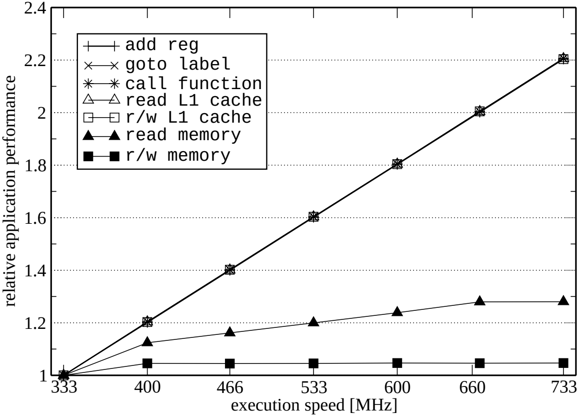
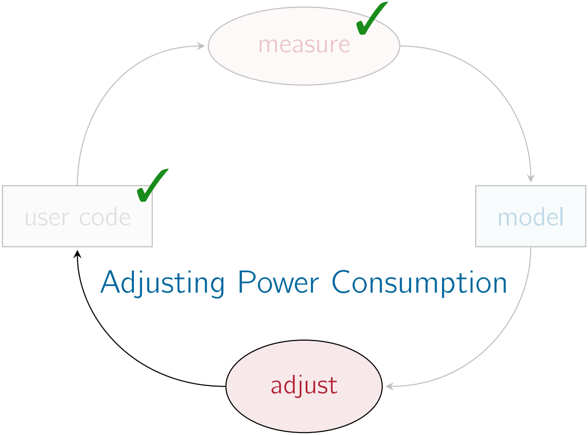


Figure: Normalized performance at different clock speeds. From [WB02].

Outline



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- **Dynamic voltage scaling**
  - Similar to DFS, but for voltage
  - Lower voltages are only available at lower clock speeds
    $\Rightarrow$ Used together with DFS as DVFS
  - DVS **affects static power consumption**
  - $E \propto V^2 \Rightarrow$ high impact!

Adjusting Power Consumption (cont'd)

- **Sleep states** (C-states)
  - $\mathrm{C}0, \mathrm{C}1, \ldots, \mathrm{C}3$, more depending on hardware
  - Higher number: lower energy usage
  - $\mathrm{C}0$: executing instructions
  - $\mathrm{C}1$: `hlt`
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- **Switching overhead**
  - Switching to and from a power saving configuration takes significant time
  - Rule of thumb: **higher savings** $\Leftrightarrow$ **higher switching time**
  - Prediction problem: Will switching save energy?

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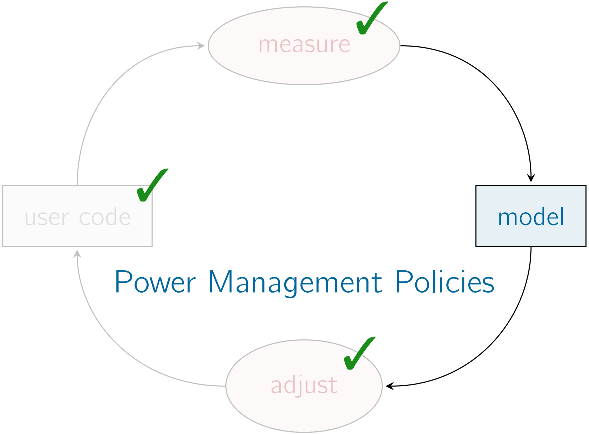

Managing Power: Policies

- Event counters span multidimensional space
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- **Maximum degradation** policy
  - minimize P subject to $pT \leq T_{\text{opt}}$
  - i.e., **minimize power consumption** P,
    but only **up to a performance loss** of $(1 - p)$ %
  - Weißel et al.: $p = 0.9$ works well, up to 37 % saved

Managing Power: Policies (cont'd)

- **Generalized energy-delay** policy
  - minimize $P^{1-\alpha} \cdot T^{1+\alpha}, \alpha \in [-1; 1]$
  -

α	policy behavior
1	maximum performance, race-to-halt
0	minimize energy usage (remember $E := \int_T P = \bar{P}T$)
-1	minimize power consumption
$0 < \alpha < 1$	throttle depending on the workload

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- Adjustable policies
  - Note the parameters!
  - **User experience matters**, user-adjustable policies help

Generalized Energy Delay

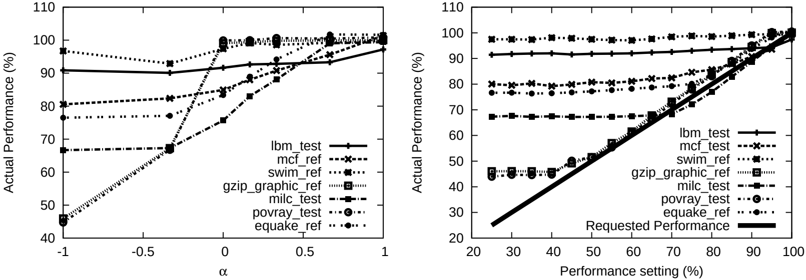

Figure: Generalized energy-delay policy. From [SLSPH09].

Challenges: Is It Really That Simple?

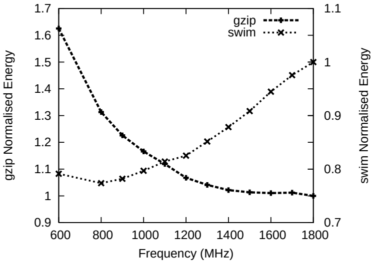

Figure: Normalized energy consumption of two benchmarks. From [SLSPH09].

- **Quality of workload prediction**
  - Bad analysis → wrong power saving decision
  - Bad prediction → sleep state overhead

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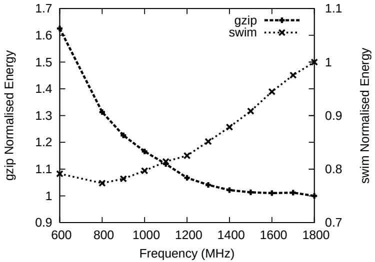

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- **Quality of workload prediction**
  - Bad analysis → wrong power saving decision
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- **Multiple and dependent variables**
  - Multiple adjustable values → more test data required
  - Snowdon et al.: memory performance depends on CPU frequency
  - Not all effects are measurable using event counters

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- Power-supply efficiency and temperature

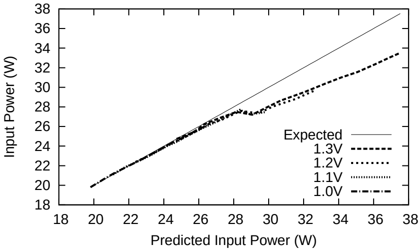

Figure: Actual vs. predicted input power of a Dell Latitude D600. From [SLSPH09].

  - Power-supply efficiency doesn't necessarily scale linearly
  - Influence of temperature (on efficiency, power required for cooling)

Notes on Implementation

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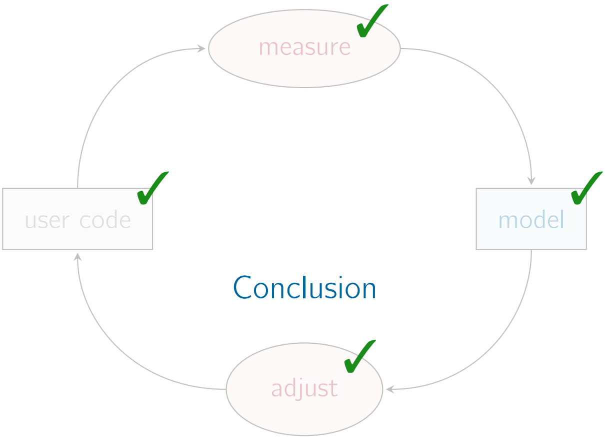

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  - involves **hardware-specific**s
- There is no free lunch: **Performance** $\leftrightarrow$ **Energy**
- Manufacturers also providing the OS are at advantage
- **Lessons learned:** write predictable applications

Q&A Session

Questions & Answers

Thank you for your attention.

References

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